disable node **516**. When the voltage difference between enable/disable signal and output node **514** is within the threshold voltage of a switch **530**, switch **530** is turned off and charge pump circuit **500** is enabled. When the voltage difference exceeds the threshold voltage of switch **530**, switch **530** is turned on and the voltage of output node **514** is clamped to the voltage of input node **512**. Because the output and input voltages are clamped when switch **530** is closed, charge pump circuit **500** is disabled.

[0049] FIG. **6** is a simplified diagram showing timing diagrams of the control signals **612***a-d* applied to control nodes **522***a-d* of charge pump circuit **500**, respectively, during a half switching cycle. Control signals **612***a* and **612***d* are initially low, and control signals **612***b* and **612***c* are initially high. At the start of the half switching cycle, control signal **612***c* transitions from high to low. After a first time delay **622**, control signal **612***d* transitions from low to high. After a second time delay **624**, control signal **612***b* transitions from high to low. After a third time delay **626**, control signal **612***a* transitions from low to high. At the end of the half switching cycle, control signals **612***a-d* transition back to their initial values in reverse order. Control signals **612***a-d* are maintained at their initial values for the second half of the switching cycle. During the second half of the switching cycle, control signals similar to control signals **612***a-d* are applied control nodes **524***a-d* of charge pump circuit **500**, respectively.

[0050] FIG. **7** is a simplified diagram of a threshold voltage detection circuit **700** according to some examples. In accordance with some embodiments consistent with FIGS. **2** and **3**, threshold voltage detection circuit **700** may be used to implement at least a portion of controller **232** and/or logic module **310**.

[0051] Threshold voltage detection circuit **700** is coupled to PWM control node **241** to monitor the PWM control signal. The PWM control signal, as well as a delayed version of the PWM signal **710**, is routed to various logic blocks of threshold voltage detection circuit **700**, as depicted in FIG. **7**. The output of the logic operation implemented by threshold voltage detection circuit **700** is bypass mode signal **245**. Intermediate signals **732** and **734** are also indicated in FIG. **7**.

[0052] The logic blocks of threshold voltage detection circuit **700** are arranged such that bypass mode signal **282** transitions from low to high after six consecutive cycles in which the duty cycle of the PWM control signal is considered high. The duty cycle of the PWM control signal is considered high when the duration of the off period of a cycle is less than the duration of a one shot signal **720**. The duration of one shot signal **720** is determined based on the RC delay defined by resistor **722** and capacitor **724**. Accordingly, a short RC delay results in a low threshold voltage (that is, the bypass mode signal **245** transitions from low to high when the duty cycle of buck converter **200** is very close to 100% and the difference between the input and output voltage is very low) and vice versa.

[0053] FIG. **8** is a simplified diagram showing timing diagrams **810-850** corresponding to various nodes of threshold voltage detection circuit **700**. Timing diagram **810** corresponds to the PWM control signal and timing diagram **820** corresponds to one shot signal **720**. After six consecutive cycles in which the duration of the off period of the PWM control signal is less than the duration of one shot signal **720**, intermediate signal **732** (as depicted in timing diagram **830**) transitions from high to low, intermediate signal **734** (as depicted in timing diagram **840**) transitions from low to high, and bypass mode signal **245** (as depicted in timing diagram **850**) transitions from low to high. Subsequently, after six cycles in which the duration of the off period of the PWM control signal exceeds the duration of one shot signal **720**, intermediate signals **732** and **734** and bypass mode signal **245** return to their initial values.

[0054] FIG. **9** is a simplified diagram of a method **900** for transitioning between switched mode and bypass mode in a power converter according to some embodiments. According to some embodiments consistent with FIGS. **1-8**, method **900** may be used by a controller, such as controller **232**, to operate a power converter, such as buck converter **200**, when transitioning between a switching mode and a bypass mode. During the switching mode, the power converter operates at a duty cycle of less than 100% to provide an output voltage that is proportional to the input voltage. During bypass mode, a bypass switch coupled between the input and output of the power converter is closed, causing the output voltage to be clamped to the input voltage and the switching circuitry of the power converter to be bypassed. In some examples, the power converter includes an n-type high-side transistor that uses a bootstrap circuit and a high-side supply capacitor to provide a sufficiently high voltage to turn on the high-side n-type transistor during switching mode. The bootstrap circuit may be associated with a maximum duty cycle at which it is effective at charging the high-side supply capacitor.

[0055] At a process **910**, a differential voltage between the input and output terminals of the power converter is reduced. According to some embodiments, when the output voltage is initially lower than the input voltage, process **910** may include increasing the output voltage by increasing the duty cycle of the power converter. Process **910** may additionally and/or alternately include reducing the input voltage of the power converter. When the power converter is incorporated within a wireless power receiver, reducing the input voltage may include communicating wirelessly and/or over a wire with a wireless power transmitter to adjust the input voltage.

[0056] At a process **920**, when it is determined that the differential voltage between the input and output terminals has dropped below a threshold voltage, a first charge pump is enabled and the bypass switch is closed. According to some embodiments, the threshold crossing is determined using a threshold voltage detection circuit that monitors the duty cycle of the power converter, such as threshold voltage detection circuit **700**. According to some embodiments, the threshold voltage is selected to be sufficiently high so as not to exceed the maximum duty cycle of the bootstrap circuit. Meanwhile, the threshold voltage is desirably as low as possible to avoid damaging the bypass switch by turning it on in the presence of a large voltage differential across its terminals. Accordingly, the threshold voltage is selected to balance these considerations. The first charge pump, once enabled, charges the high-side supply capacitor to allow the high-side transistor to be turned on even when the duty cycle of the power converter exceeds the maximum for the bootstrap circuit. According to some embodiments, process **920** includes enabling a second charge pump for turning on the bypass switch. In some examples, the bypass switch may be turned on by another suitable mechanism. Upon completion of process **920**, the power converter is operating in bypass mode.